

# Refine Search

## Search Results -

Terms	Documents
L26 and L12 and L13	0

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JPO Abstracts Database  
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IBM Technical Disclosure Bulletins

Search:

L28

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side by side

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result set

*DB=USPT; PLUR=YES; OP=OR*

L28   L26 and l12 and l13

0   L28

L27   L26

98   L27

*DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*

L26   l25 and l23

123   L26

L25   address adj tag

3873   L25

*DB=USPT; PLUR=YES; OP=OR*

L24   L23

344   L24

*DB=PGPB,USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*

L23   l17 and L22

422   L23

L22   711/\$.ccls.

23552   L22

L21   (6629205 or 6289420).pn.

3   L21

L20   l19 and l18

2   L20

L19   ('6049856' |'6522565')!.ABPN1,NRPN,PN,TBAN,WKU.

4   L19

L18   l9 and l10 and l17

37   L18

L17   (reads or read or reading) with writ\$ with l11 with l14

800   L17

L16   l12 same l13 same l14

0   L16

L15   l12 with l13 with L14

0   L15

L14   concurrent\$ or parallel or simultaneous\$ or ("same" adj time)

4217113   L14

<u>L13</u>	.l11 near2 L10	162	<u>L13</u>
<u>L12</u>	l9 near2 L11	116	<u>L12</u>
<u>L11</u>	cache	80408	<u>L11</u>
<u>L10</u>	write near2 (portion or partial)	8145	<u>L10</u>
<u>L9</u>	read\$ near2 (portion or partial)	39945	<u>L9</u>
<u>L8</u>	l7 and l6	3	<u>L8</u>
<u>L7</u>	unaligned	3168	<u>L7</u>
<u>L6</u>	horst-\$.in.	3112	<u>L6</u>
<u>L5</u>	0365281.pn.	1	<u>L5</u>
<u>L4</u>	ep 0 365 281	17475744	<u>L4</u>
<u>L3</u>	('ep365281')!.ABPN1,NRPN,PN,TBAN,WKU.	0	<u>L3</u>
<u>L2</u>	('ep0365281')!.ABPN1,NRPN,PN,TBAN,WKU.	0	<u>L2</u>
<u>L1</u>	6289420.pn.	2	<u>L1</u>

END OF SEARCH HISTORY

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(concurrent <or> simultaneous <or> parallel) <and> real

Search

☐ Check to search within this result set

## Results Key:

**JNL** = Journal or Magazine    **CNF** = Conference    **STD** = Standard

### 1 RAPID-Cache-A reliable and inexpensive write cache for high performance storage systems

*Yiming Hu; Nightingale, T.; Qing Yang;*

Parallel and Distributed Systems, IEEE Transactions on , Volume: 13 , Issue: 3 , March 2002

Pages:290 - 307

[Abstract] [PDF Full-Text (1188 KB)] IEEE JNL

### 2 A cache coherence scheme suitable for massively parallel processors

*Baldwin, R.;*

Supercomputing '93. Proceedings , 15-19 Nov. 1993

Pages:730 - 739

[Abstract] [PDF Full-Text (648 KB)] IEEE CNF

### 3 Dynamic SMP Clusters with Communication on the Fly in NoC Technology for Very Fine Grain Computations

*Tudruj, M.; Masko, L.;*

Parallel and Distributed Computing, 2004. Third International Symposium on/Algorithms, Models and Tools for Parallel Computing on Heterogeneous Networks, 2004. Third International Workshop on , 05-07 July 2004

Pages:97 - 104

[Abstract] [PDF Full-Text (224 KB)] IEEE CNF

### 4 Communication on the fly and program execution control in a system of dynamically configurable SMP clusters

*Tudruj, M.; Masko, L.;*

Parallel, Distributed and Network-Based Processing, 2003. Proceedings. Eleventh Euromicro Conference on , 5-7 Feb. 2003

Pages:67 - 74

[Abstract] [PDF Full-Text (465 KB)] IEEE CNF

### 5 Cache coherence in a multiport memory environment

*Crawford, S.E.; DeMara, R.F.;*

Massively Parallel Computing Systems, 1994., Proceedings of the First International Conference on , 2-6 May 1994

Pages:632 - 642

[[Abstract](#)] [[PDF Full-Text \(800 KB\)](#)] IEEE CNF

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**6 Global address space, non-uniform bandwidth: a memory system performance characterization of parallel systems**

*Stricker, T.; Cross, T.;*

High-Performance Computer Architecture, 1997., Third International Symposium on , 1-5 Feb. 1997

Pages:168 - 179

[[Abstract](#)] [[PDF Full-Text \(1292 KB\)](#)] IEEE CNF

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**7 Massively parallel algorithms for trace-driven cache simulations**

*Nicol, D.M.; Greenberg, A.G.; Lubachevsky, B.D.;*

Parallel and Distributed Systems, IEEE Transactions on , Volume: 5 , Issue: 8 , Aug. 1994

Pages:849 - 859

[[Abstract](#)] [[PDF Full-Text \(1000 KB\)](#)] IEEE JNL

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**8 A memory to read out and write a block of words via one memory access and its application to increase processor and cache performance**

*Polkovnikov, I.;*

Signals, Systems and Computers, 1992. 1992 Conference Record of The Twenty-Sixth Asilomar Conference on , 26-28 Oct. 1992

Pages:66 - 70 vol.1

[[Abstract](#)] [[PDF Full-Text \(328 KB\)](#)] IEEE CNF

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**9 On some implementation issues for value prediction on wide-issue ILP processors**

*Sang-Jeong Lee; Pen-Chung Yew;*

Parallel Architectures and Compilation Techniques, 2000. Proceedings. International Conference on , 15-19 Oct. 2000

Pages:145 - 156

[[Abstract](#)] [[PDF Full-Text \(1048 KB\)](#)] IEEE CNF

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**10 Reducing ownership overhead for load-store sequences in cache-coherent multiprocessors**

*Nilsson, J.; Dahlgren, F.;*

Parallel and Distributed Processing Symposium, 2000. IPDPS 2000. Proceedings. 14th International , 1-5 May 2000

Pages:684 - 692

[[Abstract](#)] [[PDF Full-Text \(172 KB\)](#)] IEEE CNF

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**11 The SPEED cache coherence protocol for an optical multi-access interconnect architecture**

*Joon-Ho Ha; Pinkston, T.M.;*

Massively Parallel Processing Using Optical Interconnections, 1995., Proceedings of the Second International Conference on , 23-24 Oct. 1995

Pages:98 - 107

[[Abstract](#)] [[PDF Full-Text \(820 KB\)](#)] IEEE CNF

---

**12 Cache memory design for the data transport to array processors**

*Volkers, H.; Jeschke, H.; Wehberg, T.;*

Circuits and Systems, 1990., IEEE International Symposium on , 1-3 May 1990

Pages:49 - 52 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(376 KB\)\]](#) [IEEE CNF](#)

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**13 The impact of negative acknowledgments in shared memory scientific applications**

*Mainak Chaudhuri; Heinrich, M.;*

Parallel and Distributed Systems, IEEE Transactions on , Volume: 15 , Issue:

2 , Feb 2004

Pages:134 - 150

[\[Abstract\]](#) [\[PDF Full-Text \(1831 KB\)\]](#) [IEEE JNL](#)

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**14 A 32Kb SRAM cache using current mode operation and asynchronous wave-pipelined decoders**

*Wieckowski, M.; Margala, M.;*

SOC Conference, 2004. Proceedings. IEEE International , 12-15 Sept. 2004

Pages:251 - 254

[\[Abstract\]](#) [\[PDF Full-Text \(328 KB\)\]](#) [IEEE CNF](#)

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**15 A 16 MB cache DRAM LSI with internal 35.8 GB/s memory bandwidth for simultaneous read and write operation**

*Nakayama, M.; Sakakibara, H.; Kusunoki, M.; Kurita, K.; Yokoyama, Y.; Miyaoka, S.; Koike, J.; Tamba, N.; Kobayashi, T.; Kume, M.; Sawamoto, H.; Kawata, A.; Tanaka, H.; Takada, Y.; Yamamoto, M.; Yagyu, M.; Tsuchiya, Y.; Yoshida, H.; Kitamura, N.; Yamaguchi, K.;*

Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2000

IEEE International , 7-9 Feb. 2000

Pages:398 - 399, 472-3

[\[Abstract\]](#) [\[PDF Full-Text \(363 KB\)\]](#) [IEEE CNF](#)

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